

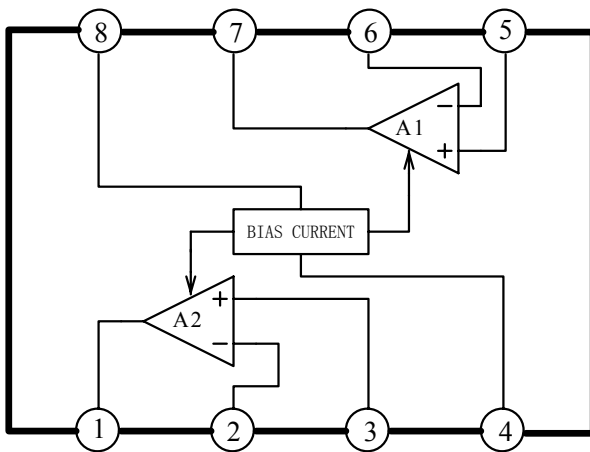
## 1. Overview

The V4558M is a dual operational amplifier designed for use as ripple filter, compensation amplifier, audio pre-amplifier and linear amplifier in electronic devices. Its features are:

- Built-in phase compensation circuit
- Low noise:  $V_{NI} = 2.5\mu\text{V}$
- Wide bandwidth and high speed,  $\text{BW} = 3\text{MHz}$
- SOP8

## 2. Block Diagram and Pin Description

### 2.1 Block Diagram



### 2.2 Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	OUT <sub>1</sub>	Output 1	5	IN <sub>2+</sub>	Positive Input 2
2	IN <sub>1-</sub>	Negative Feedback1	6	IN <sub>2-</sub>	Negative Input 2
3	IN <sub>1+</sub>	Positive Input 1	7	OUT <sub>2</sub>	Output 2
4	V <sub>EE</sub>	V <sub>EE</sub>	8	V <sub>CC</sub>	V <sub>CC</sub>

## 3. Electrical Characteristics

### 3.1 Absolute Maximum Ratings

Unless otherwise specified,  $T_{\text{amb}} = 25^\circ\text{C}$

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{CC}/V_{EE}$	$\pm 18$	V
Input Differential Voltage	$V_{ID}$	$\pm 30$	V
Input Common-mode Voltage	$V_{IC}$	$\pm 15$	V
Power Dissipation	$P_D$	500	mW
Operating Temperature	$T_{\text{amb}}$	-30~75	$^\circ\text{C}$
Storage Temperature	$T_{\text{stg}}$	-55~125	$^\circ\text{C}$

### 3.2 Electrical Characteristics

Unless otherwise specified,  $T_{amb}=25^{\circ}\text{C}$ ,  $V_{CC}=15\text{V}$ ,  $V_{EE}=-15\text{V}$

Parameter	Symbol	Test Conditions	Value			Unit	Figs
			Min	Typ	Max		
Supply Current	$I_{CC}/I_{EE}$			4.0	6.0	mA	4.5
Input Offset Current	$I_{IO}$			5	200	nA	4.2
Input Bias Current	$I_{IB}$			60	500	nA	4.2
Input Common-mode Voltage	$V_{IC}$		$\pm 12$	$\pm 14$		V	4.3
Max. Output Voltage	$V_{OM}$	$R_L \geq 10\text{k}\Omega$	$\pm 12$	$\pm 14$		V	4.4
		$R_L \geq 2\text{k}\Omega$	$\pm 10$	$\pm 13$		V	4.4
Output Shot Current	$I_{OS}$			40		mA	4.4
Output Sink Current	$I_{OSink}$			40		mA	4.4
Open Loop Voltage Gain	$A_{VO}$	$V_O = \pm 10\text{V}$ $R_L \geq 2\text{k}\Omega$	86	100		dB	4.7
Common-mode Rejection Ratio	CMRR	$R_S \leq 10\text{k}\Omega$	70	90		dB	4.3
Supply Voltage Rejection Ratio	$K_{SVR}$	$R_S \leq 10\text{k}\Omega$		30	150	$\mu\text{V}/\text{V}$	4.1
Input Offset Voltage	$V_{IO}$	$R_S \leq 10\text{k}\Omega$		0.5	6	mV	4.1
Slew Rate	$S_R$	$A_V=1$ $R_L \geq 2\text{k}\Omega$		1.0		V/ $\mu\text{s}$	4.6
Bandwidth	BW			3.0		MHz	4.7
Equivalent Input Noise Voltage	$V_{NI}$	$R_S=1\text{k}\Omega$ $f=30\text{Hz}\sim 30\text{kHz}$		2.5		$\mu\text{V}$	

### 4. Test Circuit

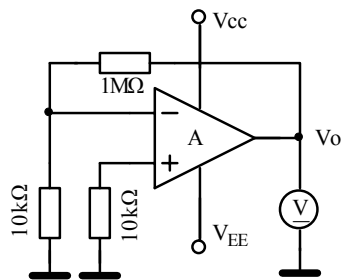


Fig 4.1

$$V_{IO}: \\ V_{IO} = V_O / 100 \quad (\text{V}) \\ K_{SVR}: \\ K_{SVR} = (V_{IO1} - V_{IO2}) / 5 \quad (\mu\text{V}/\text{V}) \\ V_{IO1}: V_{CC}=17.5\text{V}, V_{EE}=-17.5\text{V} \\ V_{IO2}: V_{CC}=12.5\text{V}, V_{EE}=-12.5\text{V}$$

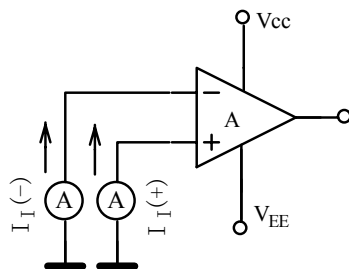


Fig 4.2

$$I_{IO}: \\ I_{IO} = | I_1(+)-I_1(-) |$$

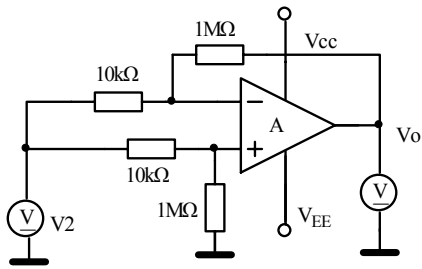


Fig 4.3

$V_{IC}$ :  
 $V_2$  is adjustable voltage,  $V_o = 1V$

$K_{CMR}$ :  
 Differential Voltage Gain to Common-mode  
 Voltage Gain Ratio

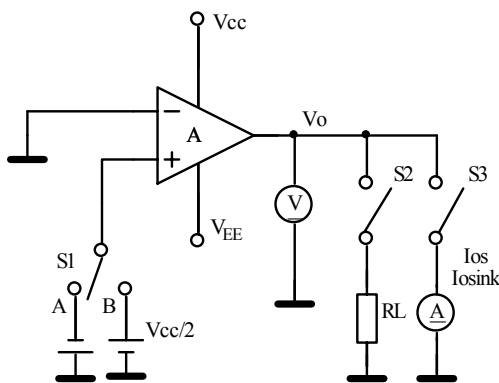


Fig 4.4

$V_{OM1+}$ :  
 $S_1=B, S_2 OFF, S_3 OFF$

$V_{OM1-}$ :  
 $S_1=A, S_2 OFF, S_3 OFF$

$V_{OM2+}$ :  
 $S_1=B, S_2 ON, S_3 OFF$

$V_{OM2-}$ :  
 $S_1=A, S_2 OFF, S_3 ON$

$I_{osink}$ :  
 $S_1=A, S_2 OFF, S_3 ON$

$I_{os}$ :  
 $S_1=B, S_2 OFF, S_3 ON$

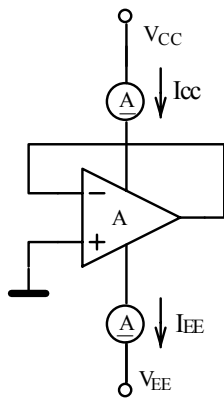


Fig 4.5

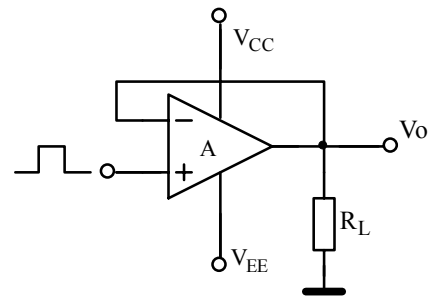
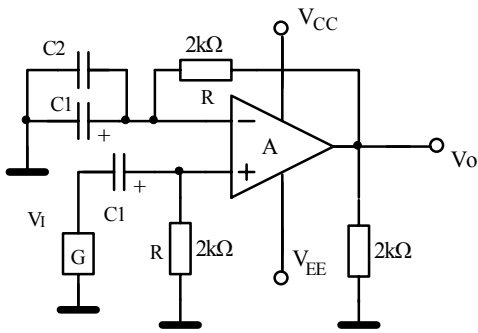


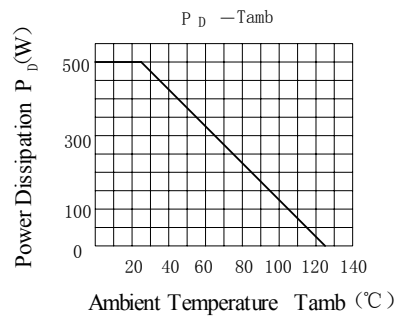
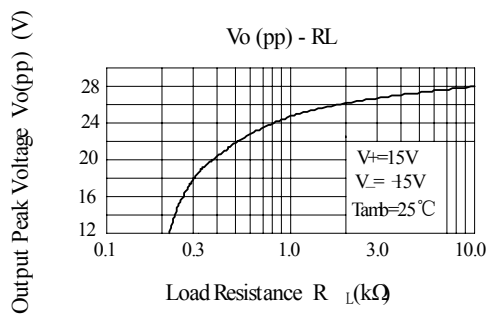
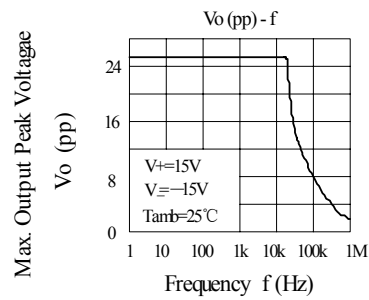
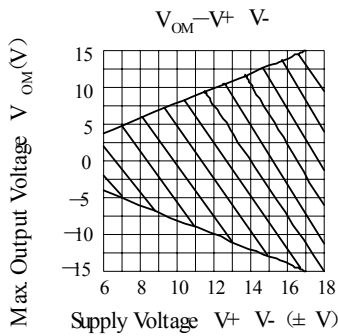
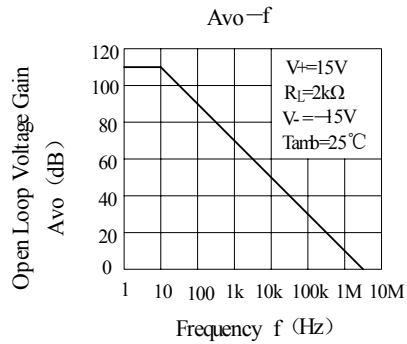
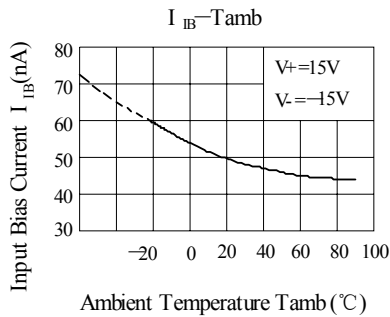
Fig 4.6



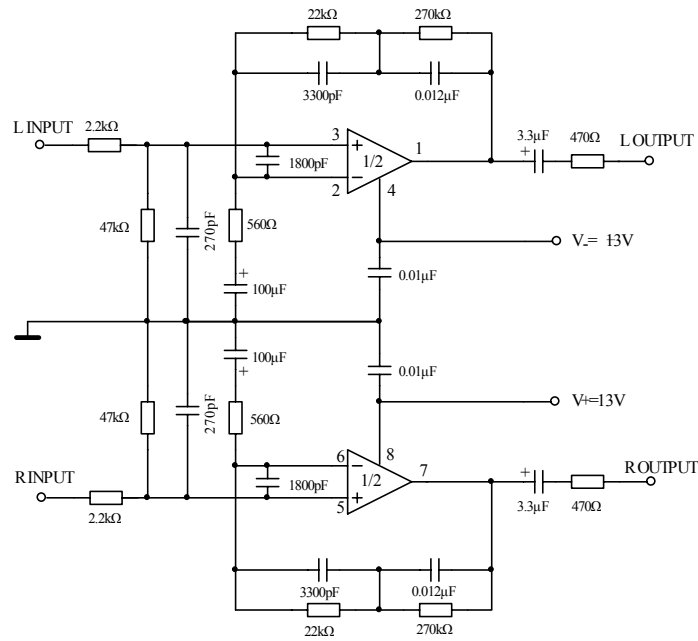
$A_{VD} = 20 \log(V_O/V_I)$   
 BW is the frequency of  $V_I$  when  $V_O = V_I$

Fig 4.7

5. Characteristics Curve



6. Application Circuit



7. Package Dimensions

