# coolaudio

# Low-Cost One-Chip Multi-Effects DSP

# V1000

#### 1. General Description

With 16 built-in reverb and multi-effects, the V1000 Digital Multi-Effects DSP delivers outstanding audio performance in a rapid time-to-market solution at a very affordable price. Since the V1000 incorporates its own RAM and on-board effects, a complete reverb system can be designed with only the V1000, a low-cost ADC and DAC, and a simple 4-bit controller such as a rotary encoder etc.

#### 2. Features

- 16 internal ROM programs consisting of effects such as multiple reverbs, echo, phaser, chorus, flanger, etc.
- Serially programmable SRAM (Writeable Control Store WCS) for program development or dynamically changing programs
- Programs run at 128 instructions per word clock. (6 MIPS @ 48 khz sampling frequency)
- 32k location Static Ram provides over 0.68 sec of delay at 48 kHz sampling frequency
- Package outline: SOIC-16/300
- ROHS compliant (PB-free)



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#### 3. Electrical Characteristics and Operating Conditions

| Parameter | Description    | Condition | Min | Тур | Max | Units |
|-----------|----------------|-----------|-----|-----|-----|-------|
| VDD       | Supply Voltage |           | 3.0 | 3.3 | 3.6 | V     |
| Idd       | Supply Current |           |     | 24  |     | mA    |
| Gnd       | Ground         |           |     | 0.0 |     | V     |
| Fs        | Sample Rate    |           | 20  | 48  |     | kHz   |

#### 4. Outputs (DigOut, SysClk, BitClk, WordClk)

| Parameter       | Description                 | Condition | Min | Тур | Max | Units |
|-----------------|-----------------------------|-----------|-----|-----|-----|-------|
| V <sub>OH</sub> | Logic "1" output<br>voltage | Unloaded  | 2.9 | _   | —   | V     |
| V <sub>OL</sub> | Logic "0" output<br>voltage | Unloaded  | _   | 0   | 0.6 | V     |

#### 5. Inputs (DigIn, Int/Ext\_, Prog0/Sdata, Prog1/SClk, Prog2, Prog3, Reset\_)

| Parameter | Description                | Condition | Min | Тур | Мах     | Units |
|-----------|----------------------------|-----------|-----|-----|---------|-------|
| VIH       | Logic "1" input<br>voltage |           | 2.0 | _   | 5.0     | V     |
| VIL       | Logic "0" input<br>voltage |           | 0.0 | _   | 0.3*Vdd | V     |

#### 6. Pin Descriptions V1000

| Pin# | Name        | PinType | Description   |
|------|-------------|---------|---|
| 1    | DigOut      | Output  | Digital serial output for stereo DAC                    |
| 2    | Int/Ext_    | Input   | Internal/external program selection                     |
| 3    | Xtalln      | Input   | 12.288 MHz crystal input                                |
| 4    | XtalOut     | Output  | 12.288 MHz crystal output                               |
| 5    | Prog0/SData | Input   | Internal program select0/serial<br>interface data line  |
| 6    | Prog1/SClk  | Input   | Internal program select1/serial<br>interface clock line |
| 7    | Prog2       | Input   | Internal program select2                                |
| 8    | Prog3       | Input   | Internal program select3                                |
| 9    | WordClk     | Output  | Word clock output                                       |
| 10   | BitClk      | Output  | Bit clock output  |
| 11   | SysClk      | Output  | System clock output                                     |
| 12   | Reset_      | Input   | Active low reset  |
| 13   | Gnd         | Ground  | Ground connection                                       |
| 14   | Vdd         | Power   | Vdd power pin   |
| 15   | NC          |         |   |
| 16   | DigIn       | Input   | Digital serial input for stereo ADC                     |

Note:

Int/Ext\_, prog0, prog1, prog2 and prog3 are pulled up to Vdd via nominal internal 30k resistor.

#### 7. Block Diagram



#### 8. Internal Programs

The SCR comes with 16 internal ROM programs ready to go. By setting the chip to internal mode, the four program pins may be used to select between the different algorithms.

| Prog[3:0] | Name                   | Description                   |
|-----------|------------------------|-------------------------------|
| 0000      | Medium                 | Reverb, Small hall (1.5 sec.) |
| 0001      | Chambr7b               | Reverb, Big hall (2.8 sec.)   |
| 0010      | Room3b                 | Reverb, Room (1.8 sec.)       |
| 0011      | Chamber2               | Reverb, Church (7 sec.)       |
| 0100      | Revers3b               | Reverb Reverse (1.2 sec.)     |
| 0101      | Gated4b                | Reverb Gated (0.8 sec.)       |
| 0110      | Room2a                 | Reverb Chapel (3 sec.)        |
| 0111      | Spring3b               | Reverb Spring (2 sec.)        |
| 1000      | Phaser1                | Phaser                        |
| 1001      | Flanger2               | Flanger                       |
| 1010      | Delay7                 | Echo                          |
| 1011      | Chorus4                | Chorus                        |
| 1100      | Earlref4               | Early Reflection              |
| 1101      | Amb4                   | Big Ambience                  |
| 1110      | Delay3                 | Stereo Delay                  |
| 1111      | Delay1 Slap-back Delay |                               |

#### 9. Programming the RAM

Alongside the 16 internal programs is an externally programmable SRAM that is easily accessible through the serial clock and data pins, by setting the chip to external mode, the SClk and SData pins become available for serial communication. Except for its external programmability, there is no functional difference between the SRAM and the internal ROMs.

#### 10. Memory Map

| Addr  |                  | Name  |                  |
|-------|------------------|-------|------------------|
|       |                  | Addr  | Name             |
| 0.127 | WCS RAM          | 0:3   | LFO Coefficients |
|       |                  | 4:127 | MAC Instructions |
| 128   | Control/Status 0 |       | ·                |

#### 11. LFO Coefficient Word

| Bit#  | Description   |        |       |  |  |
|-------|---|--------|-------|--|--|
| 31    | P: Pitch shift mode select (S must be set).   |        |       |  |  |
| 30    | S: sine/triangle select. 1:Triangle; 0: Sine.   |        |       |  |  |
|       | X[1:0]: Cross fade<br>Coefficient select. Value indicates<br>the fraction of a half sawtooth period<br>used in cross fading | X[1:0] | Xfade |  |  |
|       |   | 11     | 1/16  |  |  |
| 29:28 |   | 10     | 1/8   |  |  |
|       |   | 01     | 1/2   |  |  |
|       |   | 00     | 1     |  |  |
| 27:25 | F[12:0]: Frequency coefficient, unsigned.   |        |       |  |  |
| 14:0  | A[14:0]: Amplitude coefficient, unsigned.   |        |       |  |  |

Note:

If set, the output wave form is a sawtooth with double the triangle wave's frequency.

| Sawtooth SIN  |  |
|---------------|--|
| Sawtooth COS  |  |
| Crossfade 1   |  |
| Crossfade 1/2 |  |
| Crossfade 1/8 |  |
|               |  |

Notes:

- 1. Crossfade only used in saw tooth wave.
- 2. The sinusoid generated by the LFOs is or the formula Asin(nF / M) or Acos(nF / M), where n is the time index,  $F/M 2 \pi f/Fs$ , M is the maximum internal value, fit the selected frequency, and Fs is the sampling frequency.

Thus the frequency limits are:

 $f = (F/M) Fs/(2\pi)$ 

For triangle waves, its frequency limits are:

f = Fs /(4 Max / Increment)

= Fs /(4 0x7fffff/222\*F/M)

#### 12. MAC Instruction Word

| Bit#  | Description                                     |   |                                    |                  |  |
|-------|---|---|------------------------------------|------------------|--|
| 31    |   | S: Sign bit for   | multiplier coefficient.            |                  |  |
|       | C[7:1]: Multiplier coefficient, 2's complement. |   |                                    |                  |  |
|       | C[7:0] Chorus ins                               | truction. Only the  | e 7 MSBs are used as r             | nultiplier       |  |
|       | coefficients. The                               | LSB is used in cho  | orus mode. If I[15] is so          | et, C[7:0] is :  |  |
|       | C Description                                   |   |                                    |                  |  |
|       |   | Chorus/Xfade se   | elect                              |                  |  |
|       | 7   | 1: Pass LFO addı<br>select chorus co  | ess to address genera<br>efficient | ator &           |  |
|       |   | 0: Mask LFO add   | lress to address gene              | rator &          |  |
| 30:23 |   | select cross fade   | e coefficient.                     |                  |  |
|       | 6   | 1's com   | plement the LFO add                | ress sign bit.   |  |
|       | 5   | 1's com   | plement the LFO add                | ress sign bit.   |  |
|       | 4   | 1's c   | complement the LFO                 | address.         |  |
|       | 3   | LFO latch. 1: Latch in new LFO data; 0: Hold last<br>LFO data   |                                    |                  |  |
|       | 2:1   | LFO select.   |                                    |                  |  |
|       |   | LFO sine / cosine select.   |                                    |                  |  |
|       | 0   | 1: Cos; 0: Sin.   |                                    |                  |  |
| 22    | W: Write select.                                |   |                                    |                  |  |
|       | I[5:0]: Instruction                             | field   |                                    |                  |  |
|       | I Description                                   |   |                                    |                  |  |
| 21:16 | 5   | Chorus select (When set, MAC coefficient is LFO block output, LFO address offset added to SRAM address) |                                    |                  |  |
|       | 4   |   | Clock register C.                  |                  |  |
|       | 3   |   | Clock register B.                  |                  |  |
|       | 2   |   | Reserved – set to ze               | ro.              |  |
|       |   |   | I[1:0] Instruction                 |                  |  |
|       |   |   | 11                                 | Acc = Prod + Acc |  |
| 21:16 | 1:0   | MAC product   | 10                                 | Acc = Prod + C   |  |
|       |   | instruction   | 01                                 | Acc = Prod + B   |  |
|       |   |   | 00                                 | Acc = Prod + O   |  |
|       | A[15:0]: Mu                                     | Itiplicand address  | s. (Currently only lowe            | er 15 bits used; |  |
| 15:0  |   | reserve MSB f   | or future expansion.)              |                  |  |
|       | Address 0x0000 = LeftIn / Out;                  |   |                                    |                  |  |
|       | Address 0x0001 = RightIn / Out.                 |   |                                    |                  |  |

#### Notes:

- 1. This complement is only for the MSB, and sign-extension bits are not affected.
- 2. The LeftOut, RightOut, and C registers are in parallel with the accumulator, and will contain the same value as the accumulator if clocked at the end of the tick. Thus, a write to LeftOut or RightOut will store the current tick's results.
- 3. A write to SRAM stores the last tick's results into address A. During writes, the multiplicand is set to be the Acc, since A[15:0] is used for the excursion address. Writes to LeftOut or RightOut can use the Acc = Product + Acc instruction with the multiplier coefficient set to 0 to pass all bits unaltered.
- 4. Register B, if clocked at the end of the tick, will store the value of the current tick's multiplicand. When a read is executed, B latches LeftIn, RightIn, or SRAM. When a write is executed, B latches the accumulator from the last tick.
- 5. The accumulator contains the result from the last instruction tick, and is updated at the end of the current instruction tick.
- 6. The internal SRAM address offset automatically decrements by 1 every word clock period.
- 7. Because addresses 0x0000 and 0x0001 are being used to access the left and right channels, those SRAM memory locations may not be directly written to or read from.

| Bit # | Description   |  |  |
|-------|---|--|--|
| 31:8  | Reserved. Set to zero.  |  |  |
| 7     | M: DigOut mute in external made. Resets to 1.   |  |  |
| 6     | Z: SRAM zero. Initiates zeroing cycles until de-asserted. Resets to 0.  |  |  |
| 5     | Reserved. Set to zero.  |  |  |
| 4     | L: LFO reset pulse. Resets LFO internal status registers and clears overflow flag. Self clearing. Resets to 0.  |  |  |
| 3     | I: Instruction RAM direct mode. Resets to 1.<br>1: Instructions are written / read as soon as received; 0: Instructions<br>are written / read when the address counter rolls around to<br>matching address. |  |  |
| 2:0   | Reserved. Set to zero.  |  |  |

#### 13. Control / Status Word 0

#### 14. Instruction Set

#### LFO Declarations

The LFOs must be set up with operating parameters if you want to use them. These include amplitude and frequency coefficients, and waveform selection. The setup information for the four LFOs occupy the first four ticks in the program RAM, but the LFO setup declarations may be anywhere in the input file.

LFOn = [wav] AMP = [amp] FREQ = [freq] XFAD = [xfad]

n: LFO selection. LFOs 0 through 3 are available.

[wav]: Waveform selection. SIN: sinusoid. TRI: triangle. SAW: saw tooth.

[amp]: Waveform amplitude coefficient. ±[amp]/8 samples. 15-bit value.

[freq]: Waveform frequency coefficient. 13-bit value.

[xfad]: Cross fade coefficient selection. Choices are: 1, 1/2, 1/8, 1/16. Used for SAW waveform only.

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#### MAC mnemonic

#### **READ INSTRUCTIONS**

RZP Read, Acc = Zero + Product

RAP Read, Acc = Acc + Product

RBP Read, Acc = B Register + Product

RCP Read, Acc = C Register + Product

RZPB Read, Acc = Zero + Product, Load B register

RAPB Read, Acc = Acc + Product, Load B register

RBPB Read, Acc = B Register + Product, Load B register

RCPB Read, Acc = C Register + Product, Load B register

RZPC Read, Acc = Zero + Product, Load C register

RAPC Read, Acc = Acc + Product, Load C register

RBPC Read, Acc = B Register + Product, Load C register

RCPC Read, Acc = C Register + Product, Load C register

RZPBC Read, Acc = Zero + Product, Load B and C registers

RAPBC Read, Acc = Acc + Product, Load B and C registers

RBPBC Read, Acc = B Register + Product, Load B and C registers

RCPBC Read, Acc = C Register + Product, Load B and C registers

#### WRITE INSTRUCTIONS

WZP Write, Acc = Zero + Product

WAP Write, Acc = Acc + Product

WBP Write, Acc = B Register + Product

WCP Write, Acc = C Register + Product

WZPB Write, Acc = Zero + Product, Load B register

- WAPB Write, Acc = Acc + Product, Load B register
- WBPB Write, Acc = B Register + Product, Load B register
- WCPB Write, Acc = C Register + Product, Load B register
- WZPC Write, Acc = Zero + Product, Load C register
- WAPC Write, Acc = Acc + Product, Load C register

WBPC Write, Acc = B Register + Product, Load C register

WCPC Write, Acc = C Register + Product, Load C register

WZPBC Write, Acc = Zero + Product, Load B and C registers

- WAPBC Write, Acc = Acc + Product, Load B and C registers
- WBPBC Write, Acc = B Register + Product, Load B and C registers
- WCPBC Write, Acc = C Register + Product, Load B and C registers

#### **CHORUS** mnemonic

CHRn [MAC mnemonic] [label] [chorus controls] [optional statements]

The first three statements are required in the order given. The chorus controls and optional statements may then follow in any order, although for readability the above convention should be followed.

#### **DATA Memory Access**

The MEM instruction creates a block of memory from the free memory stack. The ABS instruction specifies one particular address, useful for buffers that only require one memory location.

**One sample of delay requires 2 memory locations**, 10 samples of delay requires 11 memory locations, etc. Memory is allocated from the free memory stack as it is requested

Examples: MEM delay 1024; 1024 location delay block. MEM buff3 0x0400; 1024 location buffer. ABS store 2; Storage location at address 2. ABS temp2 0x7FFF; Temporary storage at address 32767.

#### 15. Serial Interface Format

The basic format for the micro serial interface is:

Attn Sel R/W A7 A6 A5 A4 A3 A2 A1 A0 DN DN-1 DN-2 ... D2 D1 D0 Attn Desel

Attn : A 0-1-0 is used to signal attention / start. Sel / Desel : 0: Select; 1: Deselect. A7 – A0 : Address. R /W : 0: Read; 1: Write. DN – D0 : Data Attn Desel :Write mode only.

Notes:

1. As long as data is being send during a write, the address will be automatically incremented. Therefore only a start address need be sent.

2. The phase of the clock is unimportant.



Write Timing (Tcyc = 1/FmasterClk)



#### DigIn / DigOut Interface Format



#### 16. Mechanical Specification



|   | Dimensions (Typical) |             |  |  |  |
|---|----------------------|-------------|--|--|--|
|   | Inches               | Millimeters |  |  |  |
| А | .406"                | 10.31       |  |  |  |
| В | .295"                | 7.49        |  |  |  |
| С | .407"                | 10.34       |  |  |  |
| D | .100"                | 2.50        |  |  |  |
| Е | .008"                | 0.20        |  |  |  |
| F | .025"                | 0.64        |  |  |  |
| G | .050"                | 1.27        |  |  |  |
| Н | .017"                | 0.42        |  |  |  |
| J | .011"                | 0.27        |  |  |  |
| K | .340"                | 8.66        |  |  |  |
| L | .033"                | 0.83        |  |  |  |

Note:

Dimension "A" does not include mold flash, proportions or gate burrs.



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#### 17. Schematic Diagrams



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