coolaudio

CLASS-D AMPLIFIER DRIVER

V900

1. GENERAL DESCRIPTION

The V900 is a high-voltage, high-speed MOSFET driver with a floating PWM input, and is designed for Class-D audio amplifier applications.

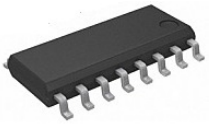
Bidirectional current sensing detects over-current conditions during positive and negative load currents without any external shunt resistors.
A built-in protection control block provides a secure protection sequence against over-current conditions and a programmable reset timer.

The internal dead-time generation block enables accurate gate switching and optimum dead-time setting for better audio performance, such as lower THD and lower audio noise floor.

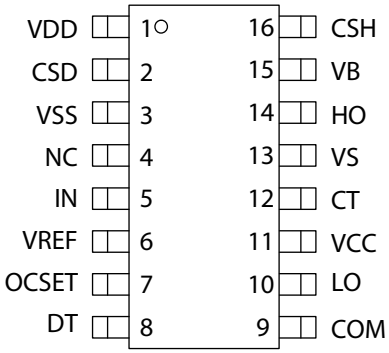
FEATURES

- Programmable constant current mode OCP timer
- Programmable preset dead-time for improved THD performances
- Programmable bidirectional over-current protection with self-reset function
- High noise immunity
- +/-100 V ratings deliver up to 500 W in output power
- 3.3 V/5 V logic compatible input
- Operates up to 800 kHz
- RoHS compliant

2. PIN CONFIGURATION



SOP16



3. TYPICAL APPLICATIONS

- Class-D amplifier driver

4. PIN DESCRIPTION

No.	Name	Functions Description	No.	Name	Functions Description
1	VDD	Floating positive supply	9	COM	Low side supply return
2	CSD	Shutdown timing capacitor, referenced to VSS	10	LO	Low side output
3	VSS	Floating supply return	11	VCC	Low side logic supply
4	NC	No Connect	12	CT	OCP timing capacitor, referenced to VCC
5	IN	PWM non-inverting input referenced to COM, in phase with HO	13	VS	High side floating supply return
6	VREF	5 V reference output for setting OCSET	14	HO	High side output
7	OCSET	Low side over-current threshold setting, referenced to COM	15	VB	High side floating supply
8	DT	Input for programmable deadtime, referenced to COM	16	CSH	High side over-current sensing input, referenced to VS

5. FUNCTIONAL BLOCK DIAGRAM

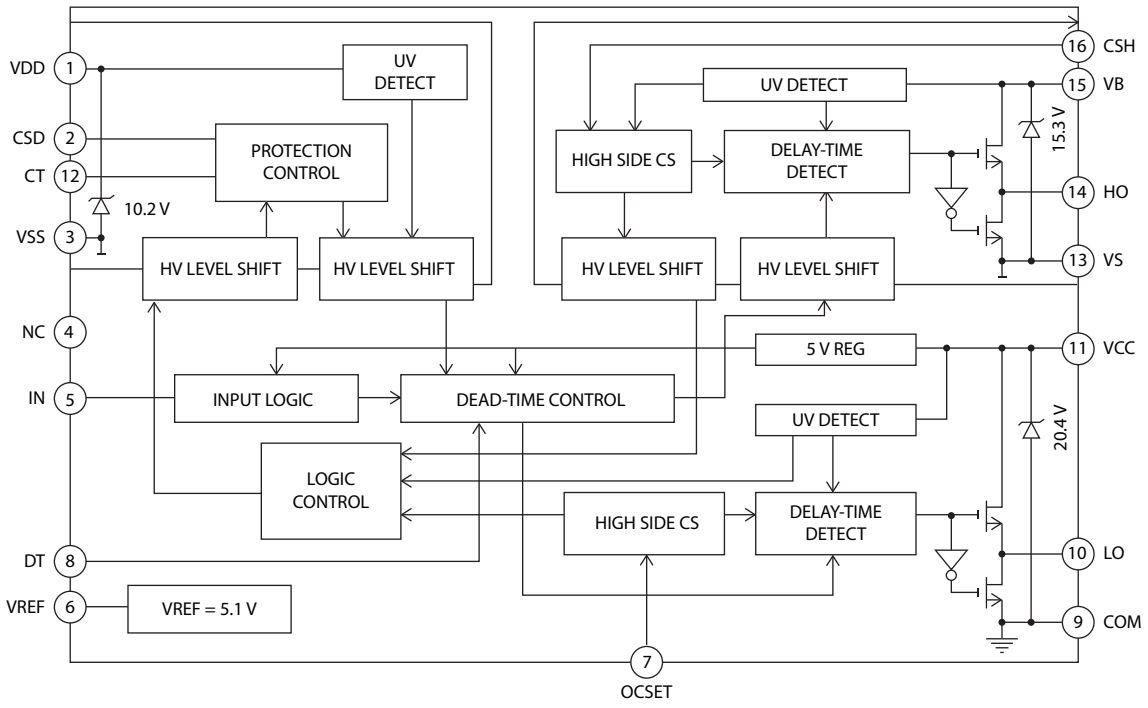


Figure 1. Functional Block Diagram

6. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min.	Max.	Unit
V_B	High side floating supply voltage	-0.3	215	V
V_S	High side floating supply voltage (1)	V_B-15	V_B+0.3	
V_{HO}	High side floating output voltage	V_S-0.3	V_B+0.3	
V_{CSH}	CSH pin input voltage	V_S-0.3	V_B+0.3	
V_{CC}	Low side fixed supply voltage (Note1)	-0.3	20	
V_{LO}	Low side output voltage	-0.3	V_{CC} +0.3	
V_{DD}	Floating input supply voltage	-0.3	210	
V_{SS}	Floating input supply voltage (Note1)	(See I_{DDZ})	V_{DD}+0.3	
V_{IN}	PWM input voltage	-0.3	V_{CC}+0.3	
V_{CT}	CT pin input voltage	-0.3	V_{CC}+0.3	
V_{CSD}	CSD pin input voltage	V_{SS} -0.3	V_{DD}+0.3	
V_{DT}	DT pin input voltage	-0.3	V_{CC} +0.3	
V_{OCSET}	OCSET pin input voltage	-0.3	V_{CC} +0.3	
V_{REF}	VREF pin voltage	-0.3	V_{CC} +0.3	
I_{DDZ}	Floating input supply zener clamp current (Note1)	—	10	mA
I_{CCZ}	Low side supply zener clamp current (Note1)	—	10	
I_{BSZ}	Floating supply zener clamp current (Note1)	—	10	
I_{OREF}	Reference output current	—	5	
dV_S/dt	Allowable VS voltage slew rate	—	50	V/ns
dV_{SS}/dt	Allowable VSS voltage slew rate (Note2)	—	50	
dV_{SS}/dt	Allowable VSS voltage slew rate upon power-up	—	50	V/ms
P_D	Maximum power dissipation	—	1.0	W
$R_{th,JA}$	Thermal resistance, Junction to ambient	—	115	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead temperature (Soldering, 10 seconds)	—	300	

Note 1: V_{DD} - V_{SS}, V_{CC} - C_{OM} and V_B - V_S contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

Note2: For the rising and falling edges of step signal of 10 V. V_{SS} = 15 V to 200 V.

7. RECOMMENDED OPERATING CONDITIONS

The device should be used within the recommended conditions below for proper operation. The V_S and COM offset ratings are tested with supplies biased at I_{DD} = 5 mA, V_{CC} = 12 V and V_B -V_S = 12 V.

Symbol	Parameter	Min.	Max.	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 18	V
V_S	High side floating supply offset voltage	(Note1)	100	
I_{DDZ}	Floating input supply zener clamp current	1	5	mA
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	18	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	PWM input voltage	0	V_{CC}	
V_{CSD}	CSD pin input voltage	V_{SS}	V_{DD}	
V_{CT}	CT pin input voltage	0	V_{CC}	—
V_{DT}	DT pin input voltage	0	V_{CC}	
I_{OREF}	Reference output current to COM (Note2)	0.3	0.8	mA
V_{OCSET}	OCSET pin input voltage	0.5	5	V
T_A	Ambient Temperature	-40	125	ºC

Note1: Logic operational for V_S equal to -5 V to +200 V. Logic state held for V_S equal to -5 V to -V_{BS}.

Note2: Nominal voltage for V_{REF} is 5 V. I_{OREF} of 0.3 mA – 0.8 mA dictates total external resistor value on V_{REF} to be 6.3 kΩ to 16.7 kΩ

8. ELECTRICAL CHARACTERISTICS

(V_{CC}, V_{BS} = 12 V, I_{DD} = 5 mA, V_{SS} = 20 V, V_S = 0 V, C_L = 1 nF and T_A = 25 °C, unless otherwise noted.)

Symbol	Test Condition	Min.	Typ.	Max.	Unit
Idle current consumption (no signal)					
I_{DD}		—	—	1.00	mA
I_{CC}		—	—	3.00	mA
I_B		—	—	1.00	mA
Current consumption (with signal)					
I_{DD}		—	0.85	—	mA
I_{CC}		—	1.80	—	mA
I_B		—	1.30	—	mA

Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vsupply zener clamp voltages					
V_{B_clamp}		14.50	15.50	16.50	V
V_{CC_clamp}		18.50	20.00	21.50	V
V_{DD_clamp}		9.50	10.00	10.60	V
V_{ref}		4.80	5.10	5.40	V
$V_{B\ UVP}$	Positive	8.35	8.85	9.35	V
	Negative	8.15	8.65	9.15	V
$V_{CC\ UVP}$	Positive	8.40	8.90	9.40	V
	Negative	8.10	8.60	9.10	V
$V_{DD\ UVP}$	Positive	8.40	8.90	9.40	V
	Negative	8.10	8.60	9.10	V
Gate driver output voltages @Vsupply = 15 V					
$H_{O\ Source\ Output}$		13.60	—	—	V
$H_{O\ Sink\ Output}$		—	—	0.10	V
$L_{O\ Source\ Output}$		13.60	—	—	V
$L_{O\ Sink\ Output}$		—	—	0.10	V
Gate driver outputs rise and fall times					
$H_{O\ Rise\ time}$		—	15.00	—	ns
$H_{O\ Fall\ time}$		—	10.00	—	ns
$L_{O\ Rise\ time}$		—	15.00	—	ns
$L_{O\ Fall\ time}$		—	10.00	—	ns
Input signal voltage thresholds					
V_{IH}		2.50	2.00	—	V
V_{IL}		—	1.80	1.50	V
V_{th1}	CSD pin shutdown release threshold	0.62 * VDD	0.7 * VDD	0.78 * VDD	V
V_{th2}	CSD pin self reset threshold	0.26 * VDD	0.3 * VDD	0.34 * VDD	V
CSD propagation delay					
T_{SD}	Enable	—	—	320.00	ns
Dead Time thresholds					
V_{DT1}	DT1 (15 ns)	51% * VCC	57% * VCC	63% * VCC	
V_{DT2}	DT2 (25 ns)	32% * VCC	36% * VCC	40% * VCC	
V_{DT3}	DT3 (35 ns)	21% * VCC	23% * VCC	25% * VCC	
Dead Time					
D_{T1}	DT1 (15 ns)	8.00	15.00	22.00	ns
D_{T2}	DT2 (25 ns)	15.00	25.00	35.00	ns
D_{T3}	DT3 (35 ns)	20.00	35.00	50.00	ns
D_{T4}	DT4 (45 ns)	25.00	45.00	60.00	ns

Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input to output propagation delay					
T_{ON_LO}	PWM turn on prop delay - LO	—	80.00	—	ns
T_{ON_HO}	PWM turn on prop delay - HO	—	80.00	—	ns
T_{OFF_LO}	PWM turn off prop delay - LO	—	65.00	—	ns
T_{OFF_HO}	PWM turn off prop delay - HO	—	65.00	—	ns
Output current drive capacity					
I_{O+_HO}	High output source current	—	1.20	—	A
I_{O-_HO}	High output sink current	—	1.80	—	A
I_{O+_LO}	Low output source current	—	1.40	—	A
I_{O-_LO}	Low output sink current	—	1.90	—	A
Output current protection					
$V_{th\ OCPH}$	High side OCP threshold in VCSH	1.0 + VS	1.2 + VS	1.4 + VS	V
$O_{CPH\ Prop\ Delay}$		—	—	500.00	ns
$O_{CPH\ Fixed\ off\ time}$		0.8	1.00	1.2	µs
$V_{th\ OCPL}$	High side OCP threshold in VCSL	1.00	1.20	1.40	V
$O_{CPL\ Prop\ Delay}$		—	—	500.00	ns
$O_{CPL\ Fixed\ off\ time}$		0.8	1.00	1.2	µs

9. TYPICAL APPLICATION CIRCUIT

Note: Please refer to Lead Assignments for correct pin configuration. This diagram shows electrical connections only.

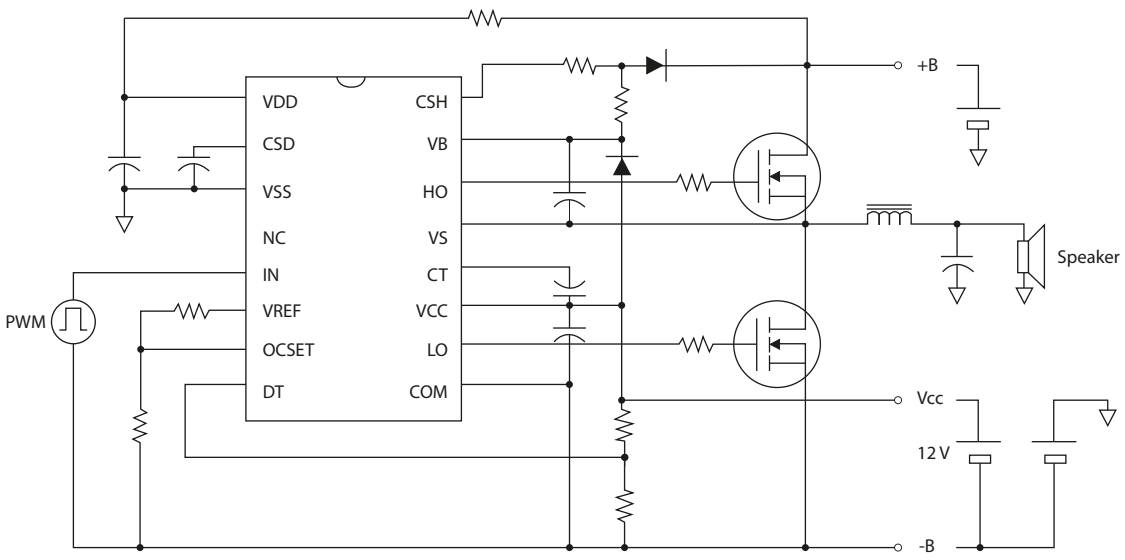
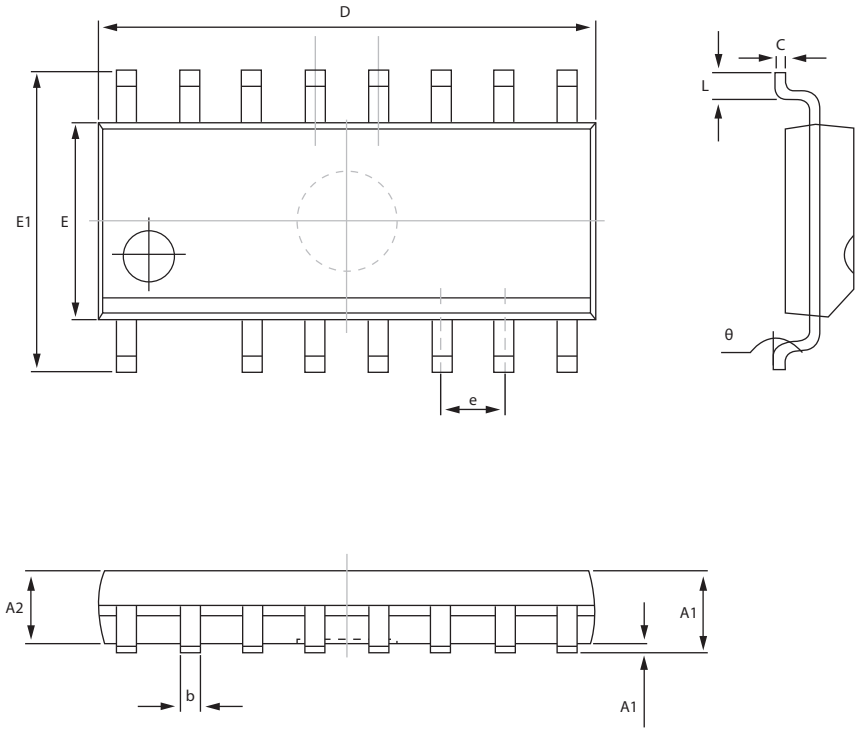


Figure 2. Typical Application Diagram

10. PACKAGE INFORMATION

S0P16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°